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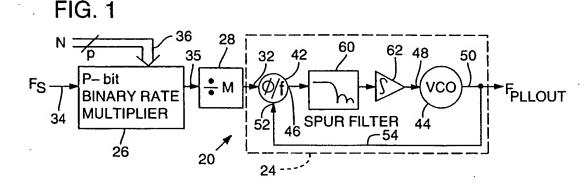
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- Phased locked loop synthesizer using a digital rate multiplier reference circuit.
- A phase locked loop synthesizer (20) for generating a digitally programmable, continuous wave signal comprises a rate multiplier (26) and divider (28) connected in a reference signal path to a phase detector (42). The rate multiplier and divider generate a reference signal which is programmable to any of a set of regularly spaced frequencies having exact decimal representations. The divider limits the

peak-to-peak phase deviation of the rate multiplier. The phase detector locks a synthesized signal generated by a variable frequency oscillator (44) to the phase of the programmed reference signal. A spur filter (60) connected to the phase detector output (46) reduces spurious frequencies in the phase detector output.





EUROPEAN SEARCH REPORT

Application Number EP 95 30 0129 1

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CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure A: member of the same patent family, corresponding					



EUROPEAN SEARCH REPORT

Application Number EP 95 30 0129

Category	Citation of document with in of relevant par		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CL6)	
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